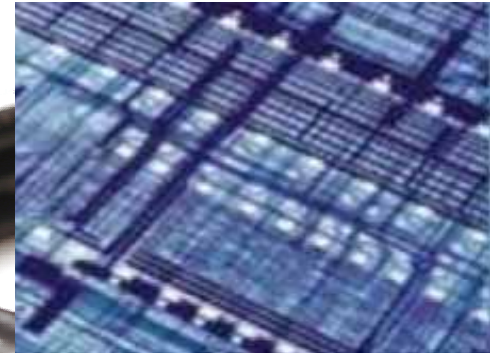


Simplify the Last DisplayPort Compliance Testing

- Tektronix DisplayPort 1.1 Test Solution





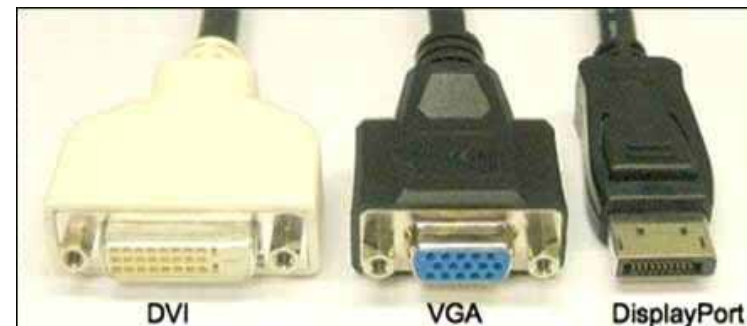
Agenda

- Introduction
- Source Testing
- Sink Testing
- Cable Testing

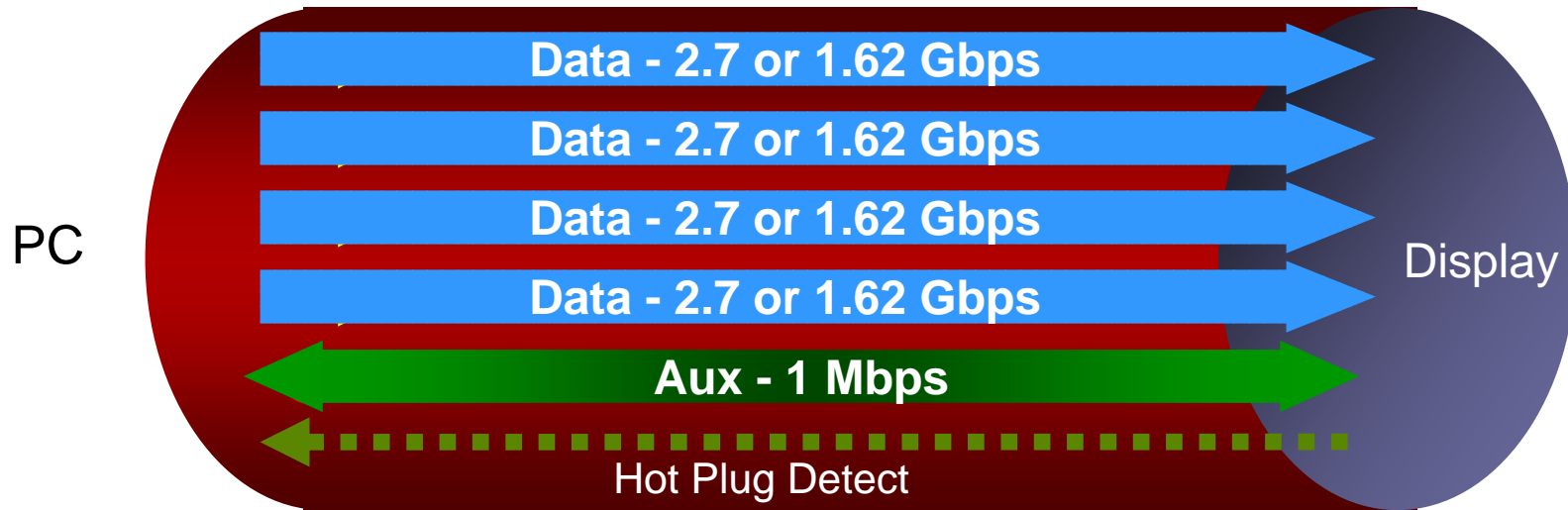
Introduction

- DisplayPort is the new digital display interface standard.
- DisplayPort will initially replace DVI interfaces in PC's. Eventually VGA.
- Promoter group consists of Dell, HP, Intel, Genesis Microchip (now ST) , NVIDIA, Samsung, ATI (now AMD), Tyco, Molex
- Benefits:
 - High Data Throughput
 - Scalable
 - Lower Cost
 - Lower Power
 - Smaller Connectors
 - etc.

 DisplayPort



DisplayPort V1.1 Technology

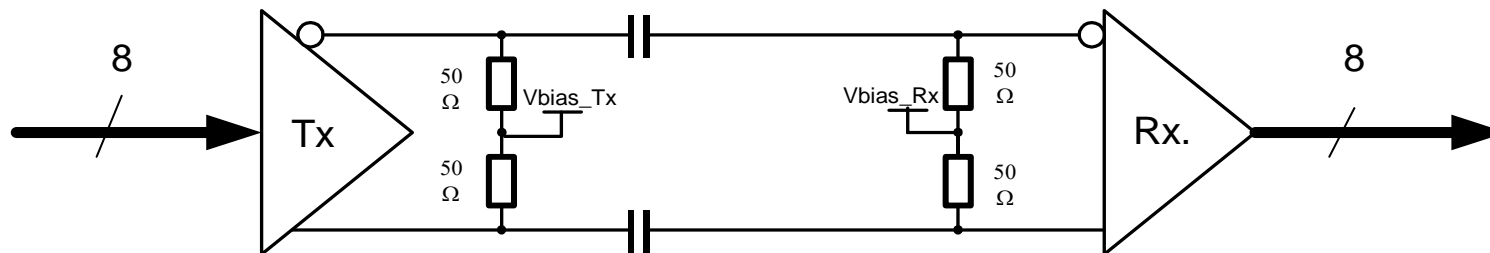


- **Scalable: 1, 2, or 4 lanes, for up to 10.8Gbps bandwidth**
 - WQXGA, 30-bit color LCDs can be supported over one link
- **Secure: HDCP 1.3 Content Protection**
- **AUX CH for 2-way communication**
- **AC-Coupled Interface**
- **Low Power, Low EMI**

Lane Width	1.6 GHz	2.7GHz
4-Lane	1080p-30bit	WQXGA-30bit
2-Lane	1080i, SXGA	WUXGA
1-Lane	XGA, SDTV	SXGA, 1080i

Structure of Main Link (Lane 0 – Lane 3)

- Consists of AC-coupled, doubly terminated differential pairs (lanes)
 - AC-coupled to facilitate semiconductor process migration



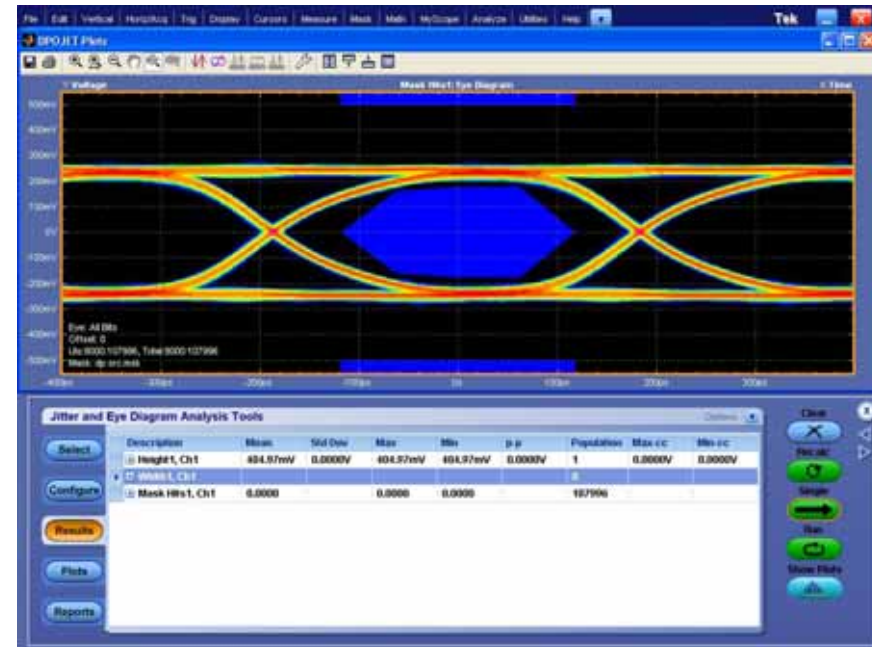
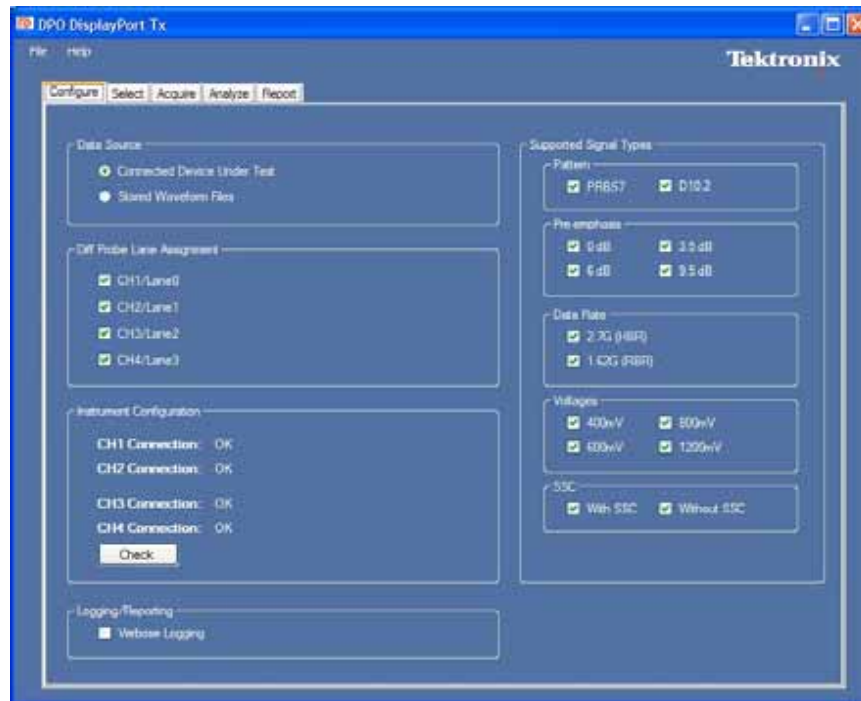
- Link rate: Either 2.7Gbps or 1.62Gbps per lane
 - “HBR” = High Bit Rate 2.7G,
 - “RBR” = Reduced Bit Rate 1.62G
 - De-coupled from Pixel Rate
 - Depends on required application bandwidth, Tx/Rx capability, and channel quality

Interoperability and Compliance Testing

- VESA publishes and maintains the standards
- Compliance test program managed by VTM
- PHY Layer Compliance Test Specification (CTS v1.0) documents officially adopted at VESA Sept. 2007
- Tektronix instruments approved for Sink, Source & Cable PHY testing by VESA February 2008
- CTS update to v1.1 – currently pending formal adoption by VESA

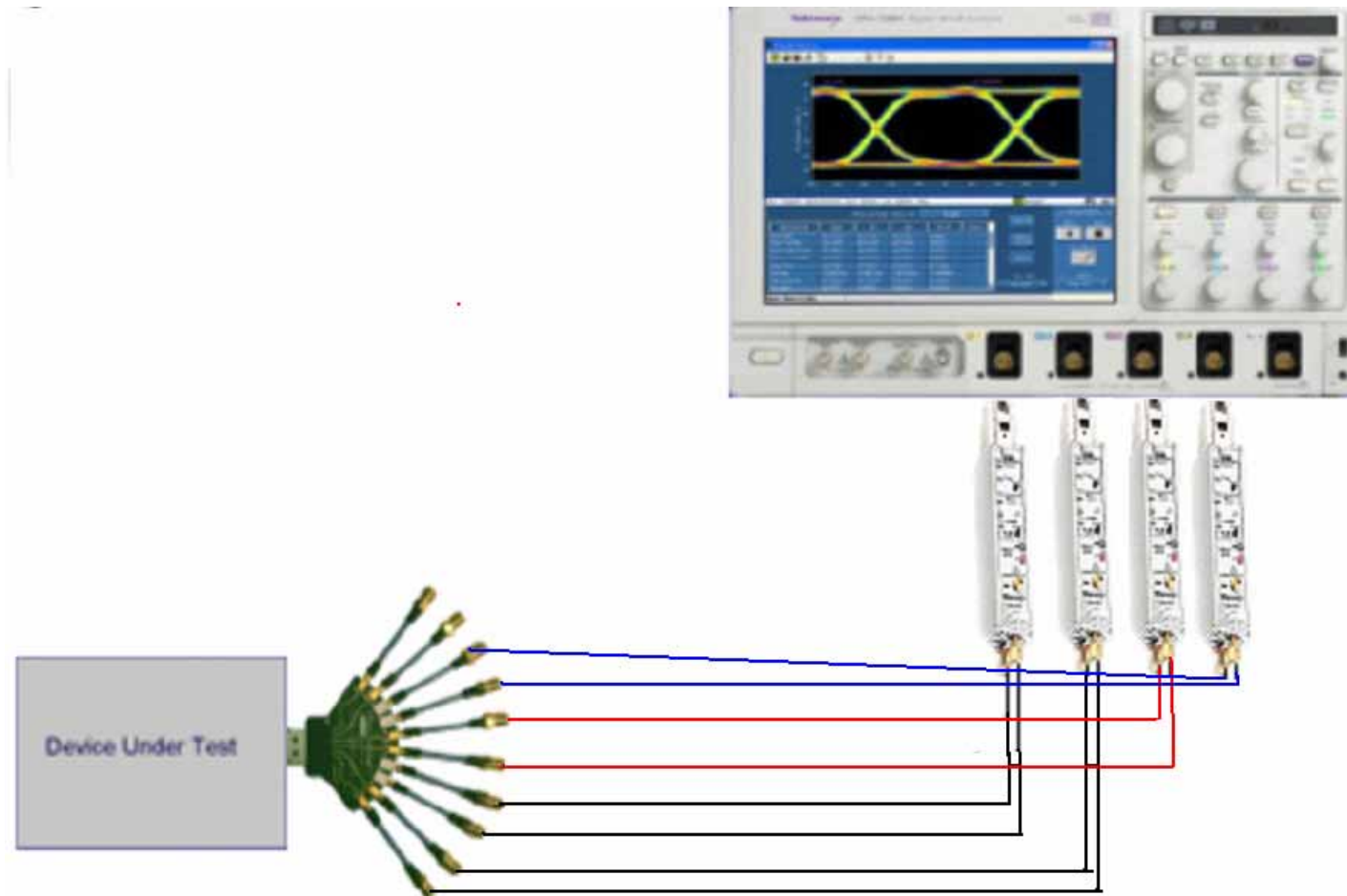


DisplayPort Source Testing



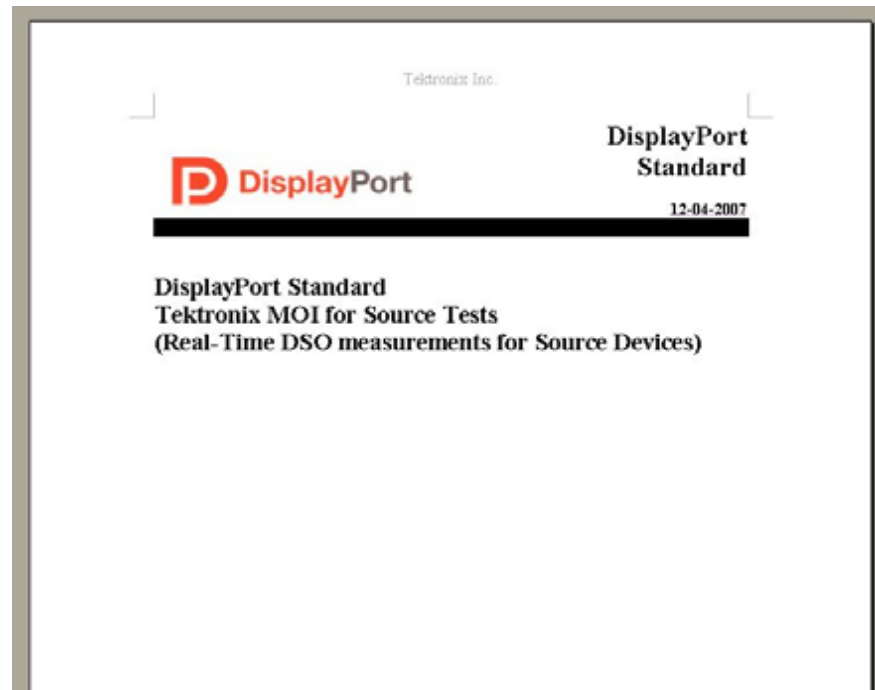
4 Lane Test with P7380SMA probes

Overall test time reduced by allowing simultaneous 4-lane acquisition & test



Tektronix DisplayPort Solutions – MOI's

- We have MOI's for Source, Sink, and Cable compliance test methods
- Submitted to VESA October 2007
- Available via www.tektronix.com/displayport



Displayport Tx Measurements

(Required for Compliance test - CTS V1.1)

- **3.1 Eye Diagram Testing (Normative)**
- **3.2 Non Pre-Emphasis Level Verification Testing (Normative)**
- **3.3 Pre-Emphasis Level Verification Testing (Normative)**
- **3.4 Inter-Pair Skew Test (Normative)**
- **3.5 Intra-Pair Skew Test (Normative)**
- *3.6 Differential Transition Time Test (Informative)*
- *3.7 Single Ended Rise and Fall Time Mismatch Test (Informative)*
- *3.8 Overshoot (Informative)*
- *3.9 Frequency Accuracy (REMOVED)*
- **3.10 AC Common Mode Noise (Normative)**
- **3.11 Non ISI Jitter Measurements (Normative)**
- **3.12 Total Jitter (TJ) Measurements (Normative)**
- *3.13 Unit Interval (Informative)*
- **3.14 Main Link Frequency Compliance (Normative)**
- **3.15 Spread Spectrum Modulation Frequency (Normative)**
- **3.16 Spread Spectrum Modulation Deviation (Normative)**
- *3.17 dF/dT Spread Spectrum Deviation HF Variation (Informative)*
- **3.18 AUX Channel DC Test (Normative)**

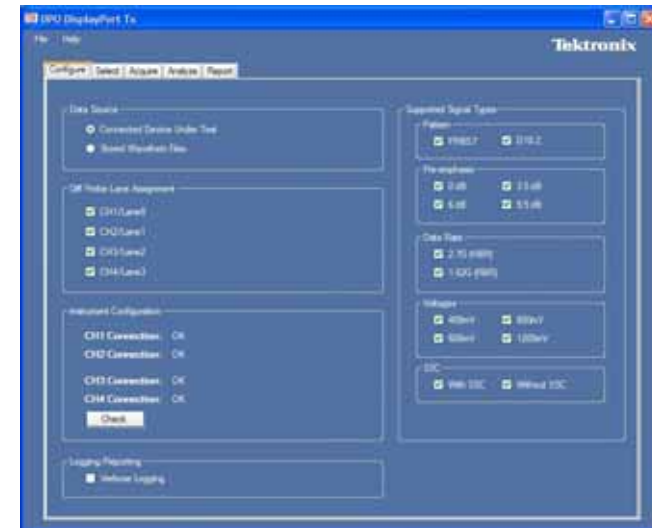
Normative – required for compliance

Informative – not required

DPO-DSPT

Compliance Automation Software

- Automates scope setup & compliance measurements per the CTS
- User-selectable DUT characteristics
- User-selectable tests
- Creates complete test report
- * Requires DPOJET



DPO-DSPT - Configure menu (Connections & device capabilities)

The screenshot displays the 'DPO DisplayPort Tx' configuration window. The 'Connect' section shows the instrument as 'GPIB8:1::INSTR' with a 'Find' button and the device ID 'DSA71604 - Q213'. The 'Data Source' section has 'Connected Instrument' selected. The 'Lane Assignment' section shows 'CH1/CH2' as 'Lane 0' and 'CH3/CH4' as 'No Connection'. The 'Instrument Configuration' section shows 'CH1 Connection: OK', 'CH2 Connection: OK', 'CH3 Connection: Not Used', and 'CH4 Connection: Not Used', with a 'Check' button. The 'Logging/Reporting' section has 'Verbose Logging' unchecked. The right panel, titled 'Supported Signal Types', lists various options with green checkmarks indicating they are supported: Pattern (PRBS7, D10.2), Pre-emphasis (0 dB, 3.5 dB, 6 dB, 9.5 dB), Data Rate (2.7G (HBR), 1.62G (RBR)), Voltages (400mV, 800mV, 600mV, 1200mV), and SSC (With SSC, Without SSC).

DPO-DSPT - Select menu

(Select tests to be run)

The screenshot shows the 'DPO DisplayPort Tx' software interface. At the top, there are menu tabs: 'Configure', 'Select', 'Acquire', 'Analyze', and 'Report'. The 'Select' tab is active. Below the tabs, there are two input fields: 'DUT Name: Unnamed DUT' and 'Comment:'. Below these is a 'Tests:' section containing a tree view of test categories and sub-items. The tree view includes:

- Tx DisplayPort Test
 - Eye Diagram Test (3.1)
 - HBR
 - RBR
 - Non Pre-emphasis Level Verification Test (3.2)
 - HBR
 - PRBS7 0dB 400mV - Math1
 - PRBS7 0dB SSC 400mV - Math1
 - PRBS7 0dB 600mV - Math1
 - PRBS7 0dB SSC 600mV - Math1
 - PRBS7 0dB 800mV - Math1
 - PRBS7 0dB SSC 800mV - Math1
 - PRBS7 0dB 1200mV - Math1
 - PRBS7 0dB SSC 1200mV - Math1
 - RBR
 - Pre-emphasis Level Verification Test (3.3)
 - Inter Pair Skew Test (3.4)
 - Intra Pair Skew Test (3.5)
 - Differential Transition Time Test (3.6) Informative
 - AC Common Mode Noise Test (3.10)
 - Non ISI Jitter Measurement Test (3.11)
 - Total Jitter (TJ) Measurement Test (3.12)
 - Unit Interval Measurement Test (3.13) Informative

At the bottom left of the 'Tests' section, there is a button labeled 'Select Only Required Compliance Tests'. Two callout boxes with arrows provide instructions: one points to the 'DUT Name' field with the text 'Enter name for Device under test', and another points to the 'Tests' list with the text 'Select tests to be run'.

DPO-DSPT - Acquire menu

(Source Device must be controlled to transmit proper signals)

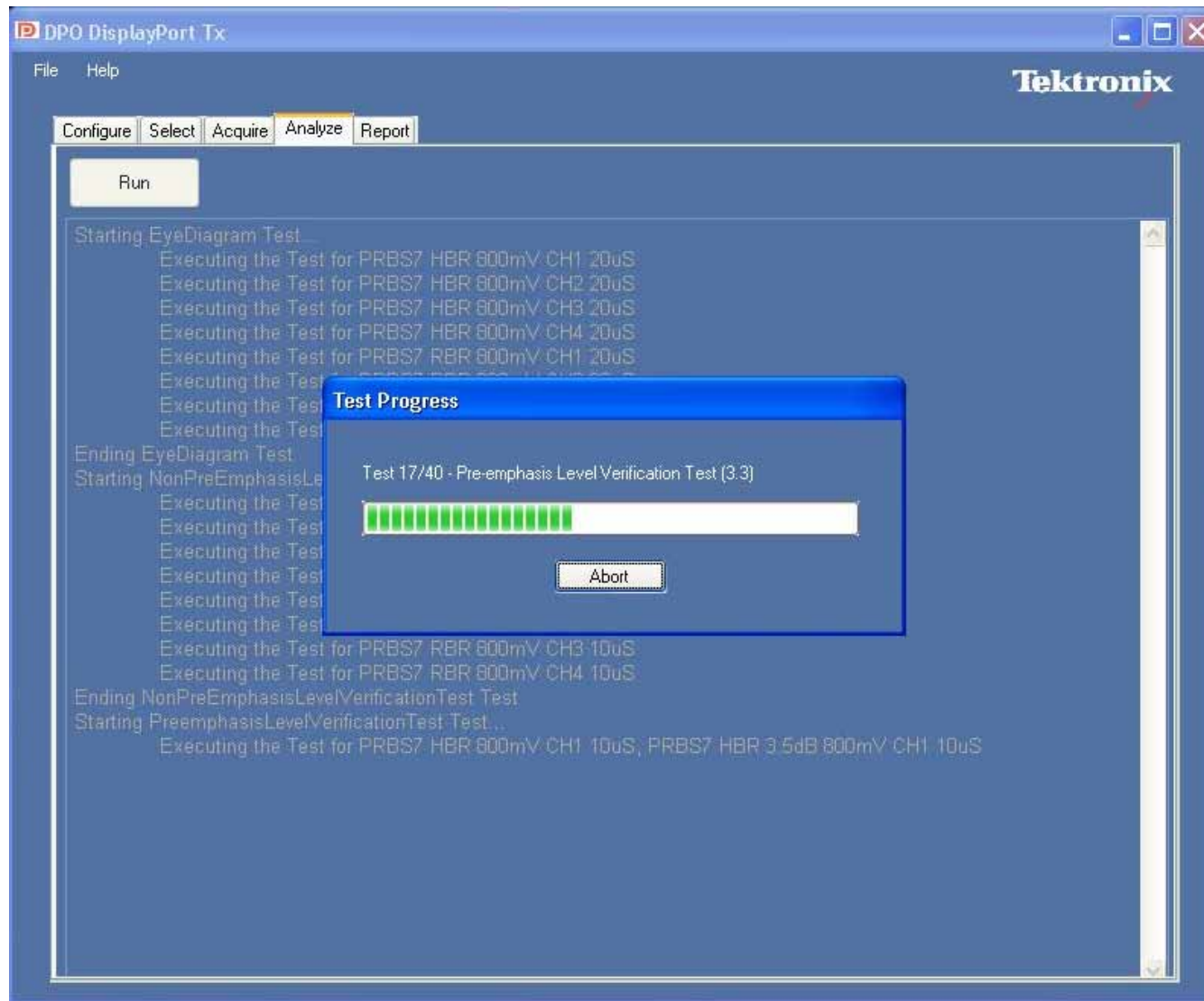
The screenshot shows the 'DPO DisplayPort Tx' software interface. The 'Acquire' menu is selected, and a 'DUT Configuration - 1/4' dialog box is open. The dialog box displays the following configuration parameters:

Parameter	Requested
Source:	CH1
Pattern:	+PRBS7
Data Rate:	2.7G
Amplitude:	800mV
Pre-emphasis:	0dB
SSC:	Disabled

The dialog box also includes buttons for 'Abort Test', 'Skip', 'Check Signal', and 'Use Signal'.

DPO-DSPT - Analyze menu

Shows progress of analysis during execution



DPO-DSPT - Report

.pdf and .csv

The screenshot shows the 'DPO DisplayPort Tx' application window. The menu bar includes 'File' and 'About'. The toolbar contains icons for printing, saving, and navigating between pages (1 / 2). The main content area displays test results for '1.3. Eye Diagram Test (3.1)'. At the top, there are two summary rows:

Non Pre-emphasis Level Verification Test (3.2)	Pass	N/A	Pass
AC Common Mode Noise Test (3.10)	Pass	N/A	Pass

Below this, the '1.3. Eye Diagram Test (3.1)' section shows a 'Result' table:

Result
Pass

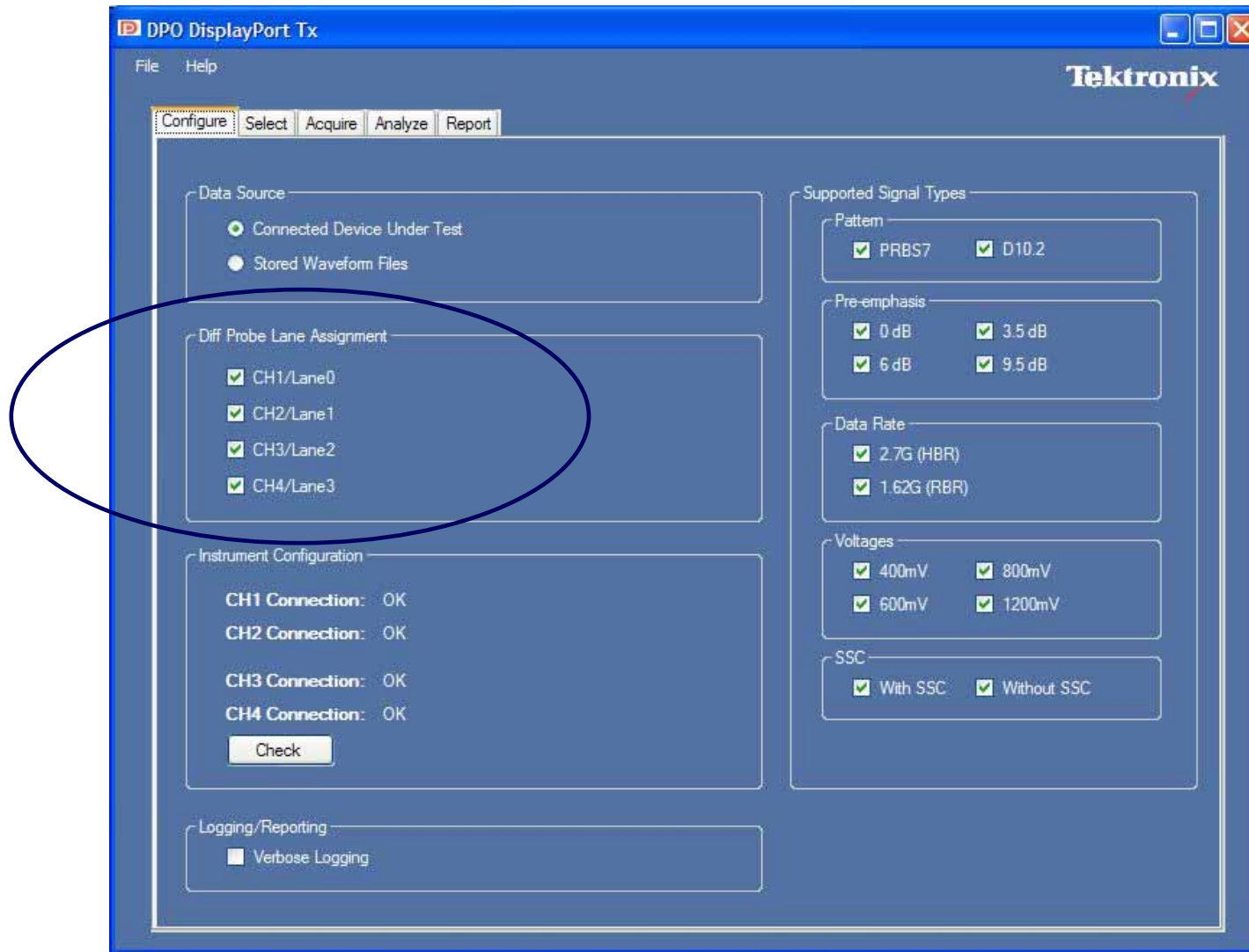
Next is a detailed table with four columns: Description, Hit Count, Status, and Plot.

Description	Hit Count	Status	Plot
HBR 800mV	0.0	Pass	

At the bottom of the window, the date and time are displayed: 'Sunday, December 02, 2007 - 4:06:37 PM'.

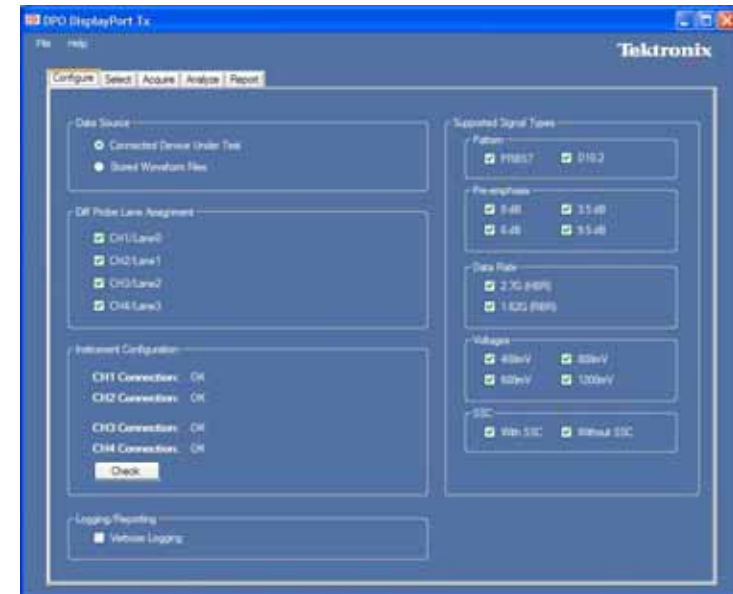
DPO-DSPT

Configure menu: 4-probe support

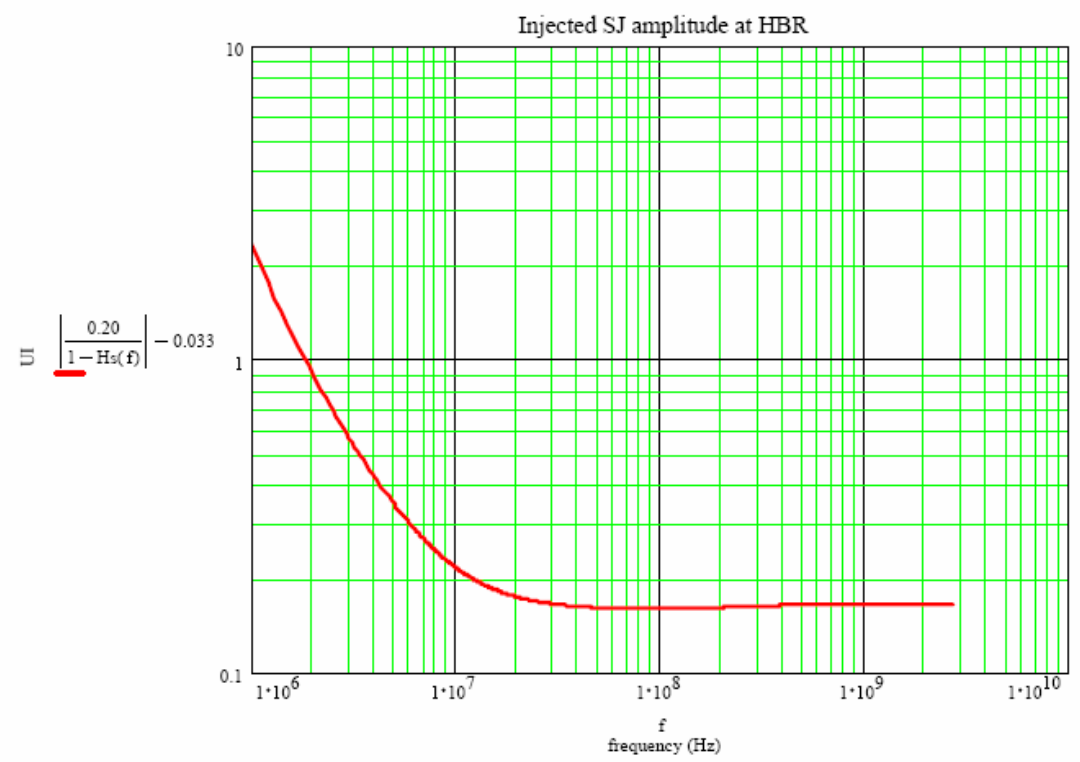


DPO-DSPT

- All waveform data saved
- Post-processing & re-test supported
- **P7380SMA - superior SMA probe**
 - Signal Fidelity advantage



DisplayPort Sink Testing



Tektronix Sink solution

AWG7122B (24GS/s)

DSA70804 or TDS6000B/C

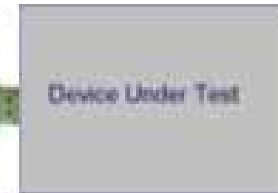
(>8GHz, jitter calibration)



Lane 1 Stressed Pattern applied on Lane under test

Lane 2 Half clock pattern on adjacent lanes

Lane 0 Half clock pattern on adjacent lanes



ET-DP-TPA-P (Plug fixture from Efficere)

Direct Synthesis with AWG

The Tektronix AWG7122B 24GS/s Arbitrary Waveform Generator is used to synthesize the TP2 impaired signals used to validate receivers are operating at the prescribed bit error rate*.

The AWG's unique strengths are in its ability to recall and play back synthesized signals which represent expressions of Sinusoidal, ISI, Rj, BUJ jitter, pre-emphasis, equalization, transition time and amplitude control with a single button press.

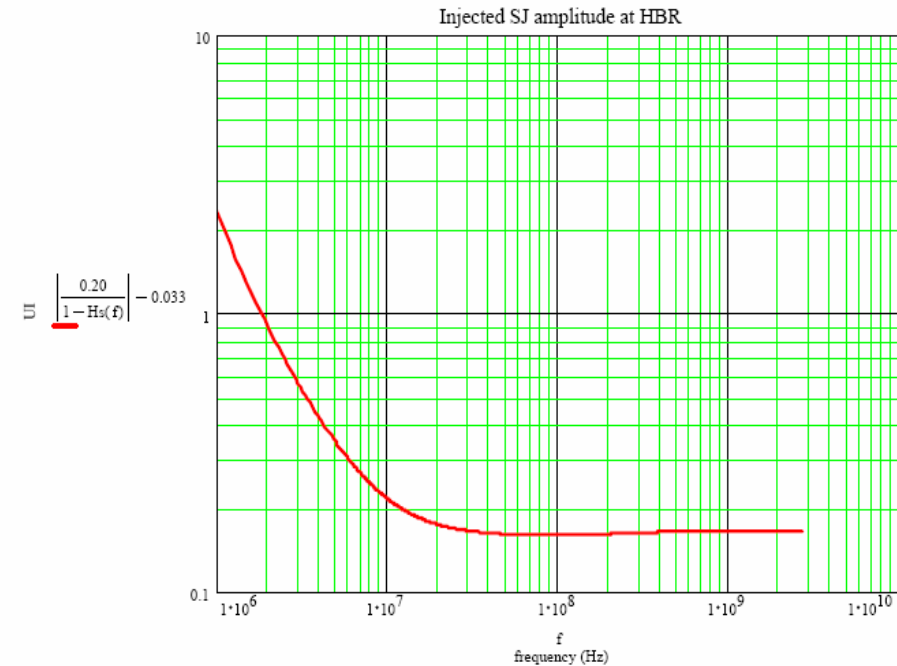
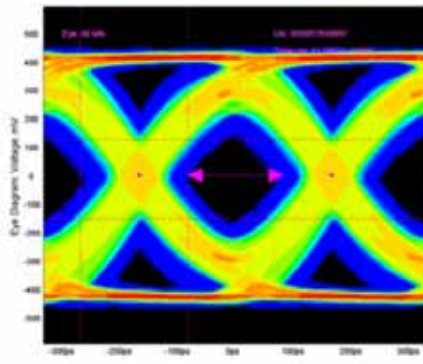


Table 4-2: Jitter Component Settings for Reduced Rate

f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	7.9	981
10	778	570	7.9	111
20	747	570	7.9	80

DP Stressed Pattern Library

1. Input File: PRBS7.txt (from DP Spec v1.1)

The screenshot shows the 'Base Pattern' configuration window. It has three tabs: 'Base Pattern', 'Transmitter', and 'Channel/Cable'. The 'Base Pattern' tab is active. Under 'Base Pattern', there are three radio buttons: 'Standard' (selected), 'From File', and 'User Pattern'. The 'From File' option is selected, with the file path 'C:\PRBS7.txt' entered. Below this, there are fields for 'Signal' (Data Rate: 2.700000000 G B/s, Amplitude: 1.000 Volts, Idle State: 12.800 n secs) and 'Encoding' (Scheme: NON, 8B10B Disp). There are also 'Rise/Fall' settings (Rise/Fall Time: 10/90, Rise: 200 p secs, Fall: 200 p).

2. Enter Sj, Rj parameters

The screenshot shows the 'Transmitter' configuration window. It has three tabs: 'Base Pattern', 'Transmitter', and 'Channel/Cable'. The 'Transmitter' tab is active. It contains sections for 'Periodic Jitter (Pk-Pk)', 'Random Jitter (RMS)', and 'SSC'.
- 'Periodic Jitter (Pk-Pk)': A table with columns for Magnitude, Frequency (Hz), and Phase (*).

	Magnitude:	Frequency (Hz):	Phase (*):
<input checked="" type="checkbox"/> Sine1:	0.981 UI	2.000000 M	0.00
<input type="checkbox"/> Sine2:	0.000 UI	10.000000 M	0.00
<input type="checkbox"/> Sine3:	0.000 UI	10.000000 M	0.00
<input type="checkbox"/> Sine4:	0.000 UI	10.000000 M	0.00

- 'Random Jitter (RMS)': A table with columns for Magnitude, Frequency-Low (Hz), and Frequency-High (Hz).

	Magnitude:	Frequency-Low (Hz):	Frequency-High (Hz):
<input checked="" type="checkbox"/> Rj1:	0.008 UI	100.000 K	500.000000 M
<input type="checkbox"/> Rj2:	0.000 UI	100.000 K	500.000000 M

- 'SSC': Includes 'Shape' (Triangle), 'Spread' (Down), 'Unequal Spread' (0.00 %), 'd/dt' (0.000 ppm/μs), 'Frequency' (4000.000 ppm), 'Modulation' (33.000 K Hz), 'Noise' (0.000 ppm), and 'Pre/De-emphasis' (0.000 dB).

DP Stressed Pattern Library

3. Enter ISI value

Base Pattern Transmitter Channel/Cable

ISI: 0.570 UI

S-Parameter Filter:

Read from File:

Inverse Filter:

ISI Scaling: 1.000

4. Compile Settings

Compile Settings

Waveform Name: DisplayPort_RBR_PRBS7_2MHz

Data Rate: 1.620000000 Gbps = Sampling Rate: 16.200000000 G S/s

Sampling Rate: 16.200000000 G S/s Automatic

Samples per UI: 10.000000000

Bandwidth Expansion Filter

Interleave Off

Interleave without Zeroing

Interleave with Zeroing

Compile Button Preferences

Compiles and Sends To

Compiles Only

Overwrite Waveform in SerialXpress List

Batch Compile

Show Graph after Compile

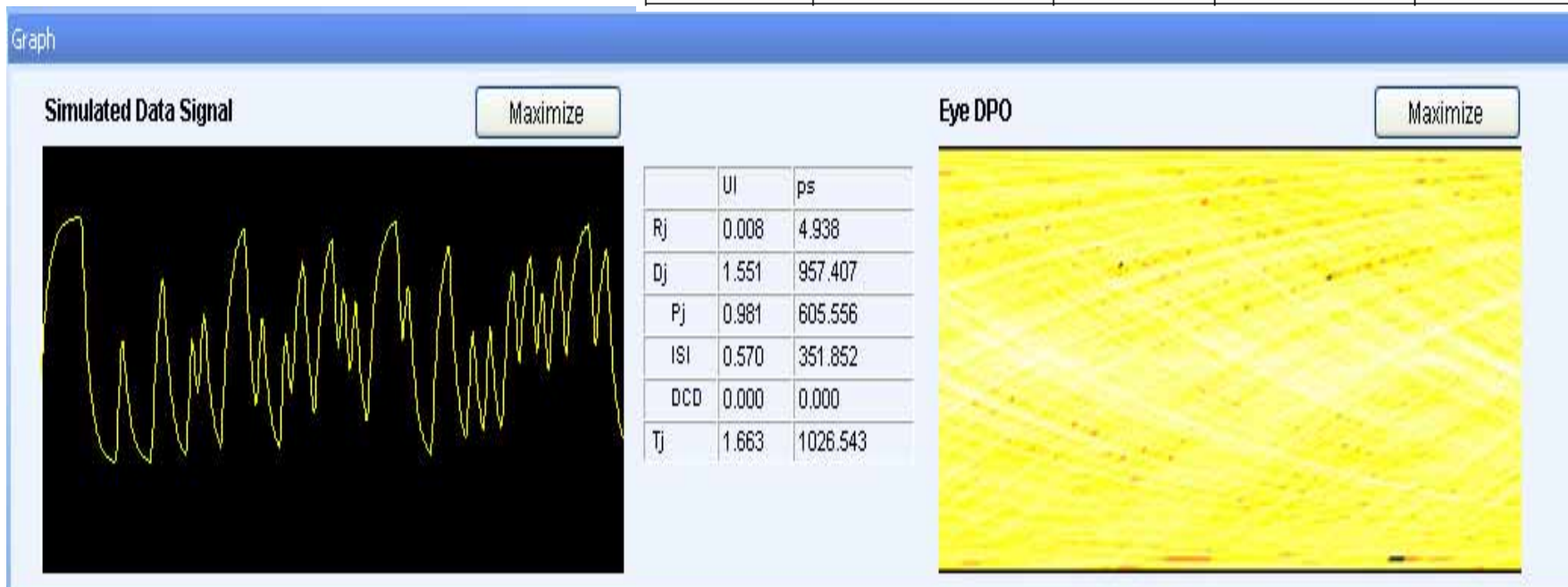
DP Stressed Pattern Library

4. Verify pattern matches requirement:

$$T_j = 1.6UI \text{ (+/- 5\%)}$$

Table 4-2: Jitter Component Settings for Reduced Rate

f(Sj)	Tj(JTRBRrx)	ISI	RJ(RMS)	SJ
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]
2	1648	570	7.9	981
10	778	570	7.9	111
20	747	570	7.9	80



Jitter Tolerance sequence

1. Frequency Lock (D10.2 => 1010)
2. Symbol Lock (K28.5, D11.6, D10.2)
3. PRBS7 then error counter cleared
4. Single bit error applied for verification
5. Error counter cleared again
6. PRBS7 output with specified R_j , S_j , and ISI
7. Run for prescribed time and verify number of bit errors

AWG7102 - Jitter_tolerance_complete.awg

File Edit View Settings Tools System Help

Sampling Rate: 16.200 000 GS/s Status: Stopped Run Mode: Sequence Force Trigger Force Event All Outputs On/Off Run

Waveform List

User Defined Predefined

Waveform Name	Length	Date
▼ D10dot2_HBR	2.93M	2007/
▼ D10dot2_RBR	2.93M	2007/
▼ prbs_1bit_error_hbr	2.93M	2007/
▼ prbs_1bit_error_rbr	4.88M	2007/
▼ prbs_hbr	2.93M	2007/
▼ prbs_hbr_100MHz	2.93M	2007/
▼ prbs_hbr_10MHz	2.93M	2007/
▼ prbs_hbr_20MHz	2.93M	2007/
▼ prbs_hbr_2MHz	2.93M	2007/
▼ prbs_rbr	4.88M	2007/
▼ prbs_rbr_10MHz	4.88M	2007/
▼ prbs_rbr_20MHz	4.88M	2007/
▼ prbs_rbr_2MHz	4.88M	2007/
▼ Symbol_Lock_HBR	2.93M	2007/
▼ Symbol_Lock_RBR	2.93M	2007/

Sequence

Total Time : ??? Current : 1 Running :

Index No	Ch 1 Waveform	Ch 2 Waveform	Wait	Repeat	Event Jump To
1	D10dot2_HBR	Empty		Infinite	Next
2	Symbol_Lock_HBR	Empty		Infinite	Next
3	prbs_1bit_error_hbr	Empty			
4	prbs_hbr_2MHz	Empty		Infinite	Next
5	prbs_hbr_10MHz	Empty		Infinite	Next
6	prbs_hbr_20MHz	Empty		Infinite	Next
7	prbs_hbr_100MHz	Empty		Infinite	Next
8	D10dot2_RBR	Empty		Infinite	Next
9	Symbol_Lock_RBR	Empty		Infinite	Next
10	prbs_1bit_error_rbr	Empty			
11	prbs_rbr_2MHz	Empty		Infinite	Next
12	prbs_rbr_10MHz	Empty		Infinite	Next
13	prbs_rbr_20MHz	Empty		Infinite	Next
14					

Waveform

Ch 1: 0.38 V Ch 2:

Δ 0 Pts C1 Pos: 0 Pts C2 Pos: 0 Pts

0.400 V

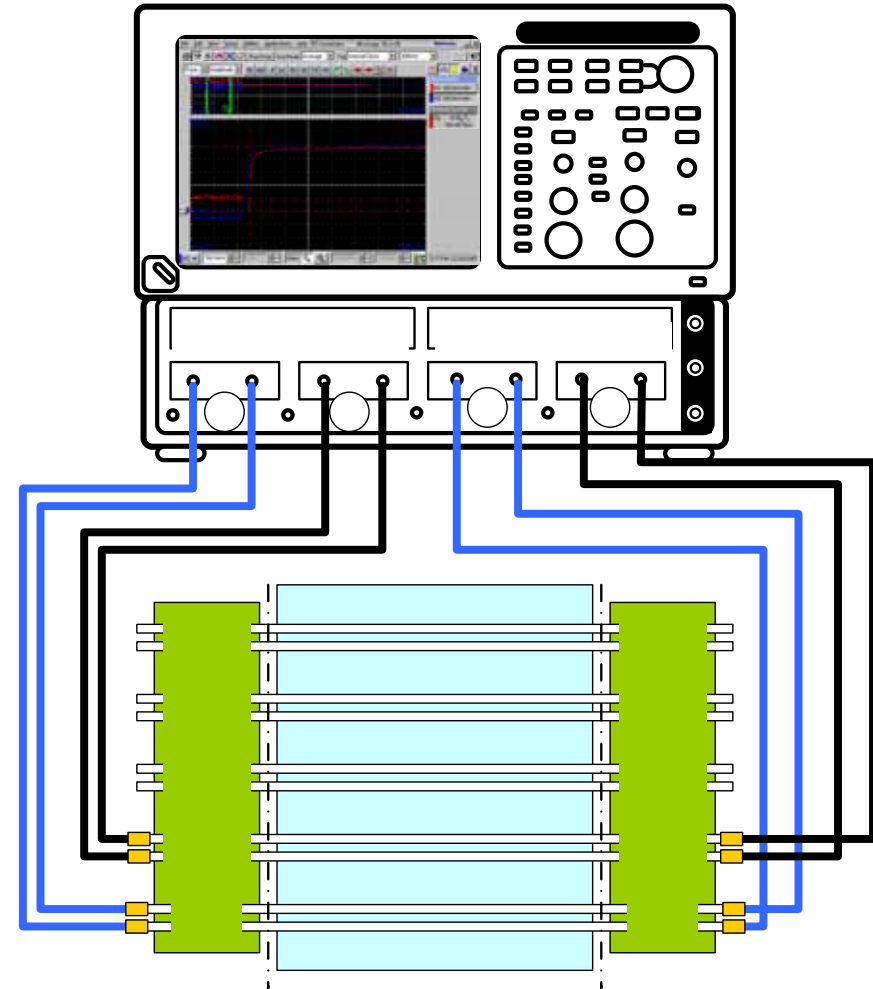
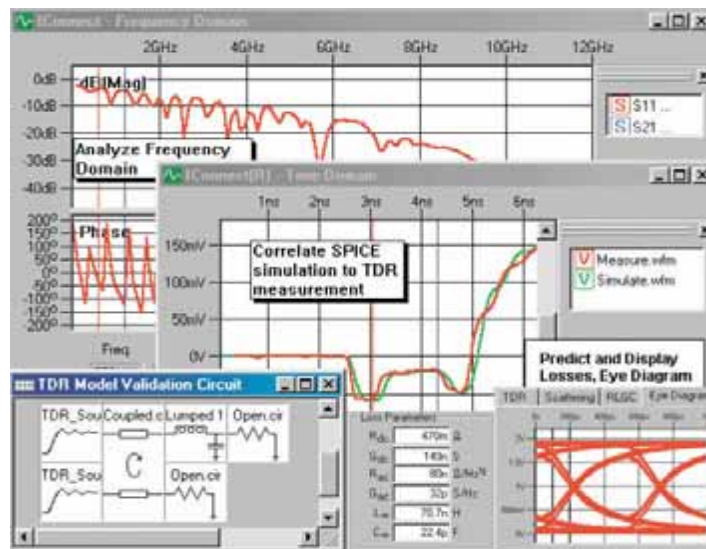


DisplayPort Cable Testing

- *5.1 Cable Assembly Inter-pair Skew Measurements (Informative)*
- *5.2 Cable Assembly Intra-pair Skew Measurements (Normative)*
- *5.3 Far End Noise (FEN) Measurements (Normative)*
- *5.4 Bulk Cable and Connector Impedance Measurements (Normative)*
- *5.5 Insertion Loss (IL/SDD21) Measurements (Normative)*
- *5.6 Near End Noise (NEN) Measurements (Normative for AUX Channel, Informative for Data Channel)*
- *5.7 Return Loss (RL/SDD11) Measurements (Normative)*

DisplayPort Cable Test Automation

- Sampling scope: DSA8200
- TDR Modules: 80E04
- IConnect software 80SSPAR
- DisplayPort test fixtures
- Cable Test MOI
- Automation script



DisplayPort Efficere Fixtures

ET-DP-TPA-S

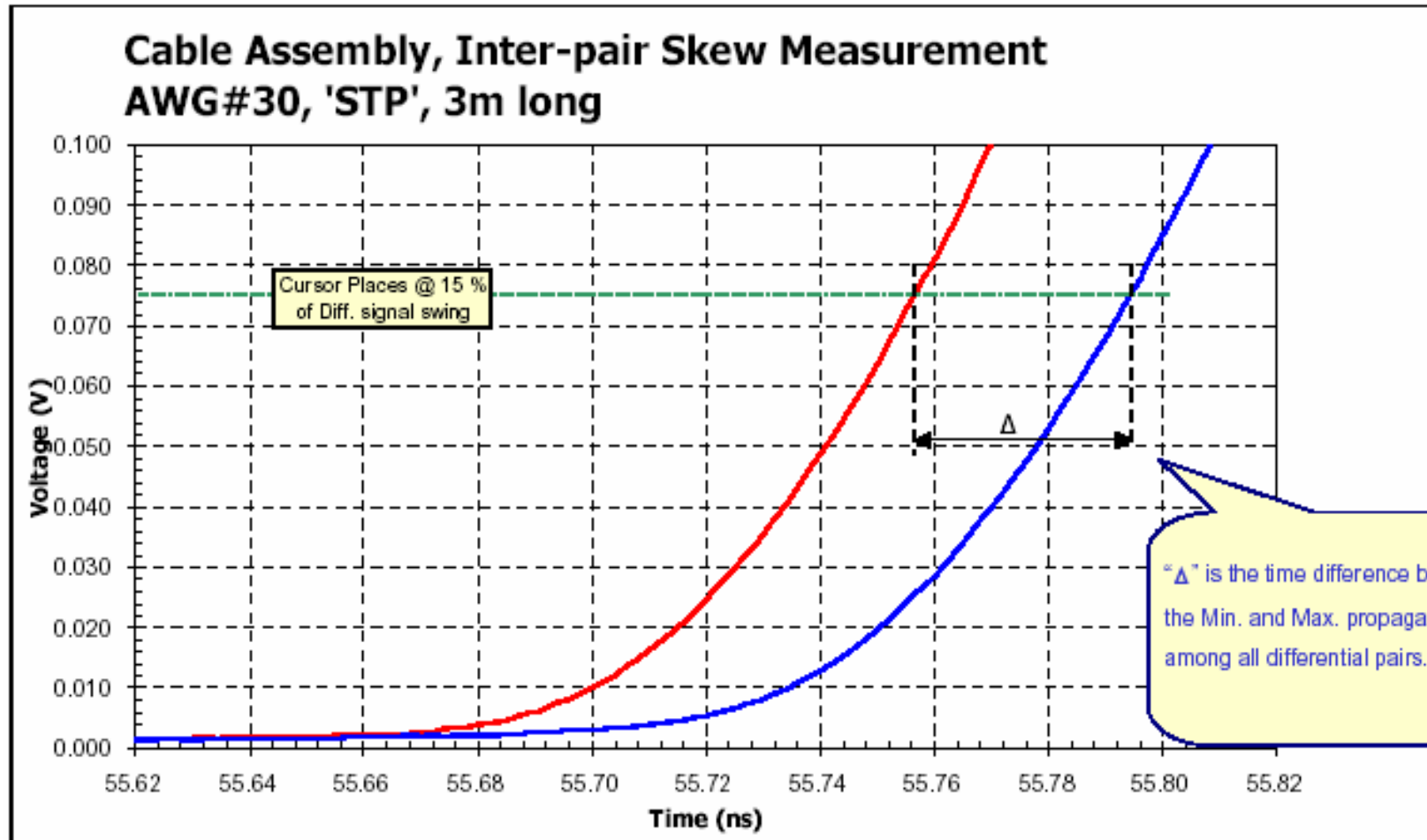
Specifications *(preliminary information)*

	Units/ Condition	Minimum	Typical	Maximum	SDR Requirement ²	DDR Requirement ²
Insertion Loss ¹	GHz at -3 dB	17.0	17.5		6.75	13.
Return Loss ¹	GHz at -20 dB	9.5	10		4.05	8.1
VSWR ¹	10 GHz	1.3:1	1.2:1			
Rise Time ¹	pS 10/90%			55		
Trace Differential Impedance ³	ohms	95	100	105		
SOLT Trace Impedance ⁴	ohms	47.5	50	52.5		
DP_Power Carrying ⁵	mA			500		

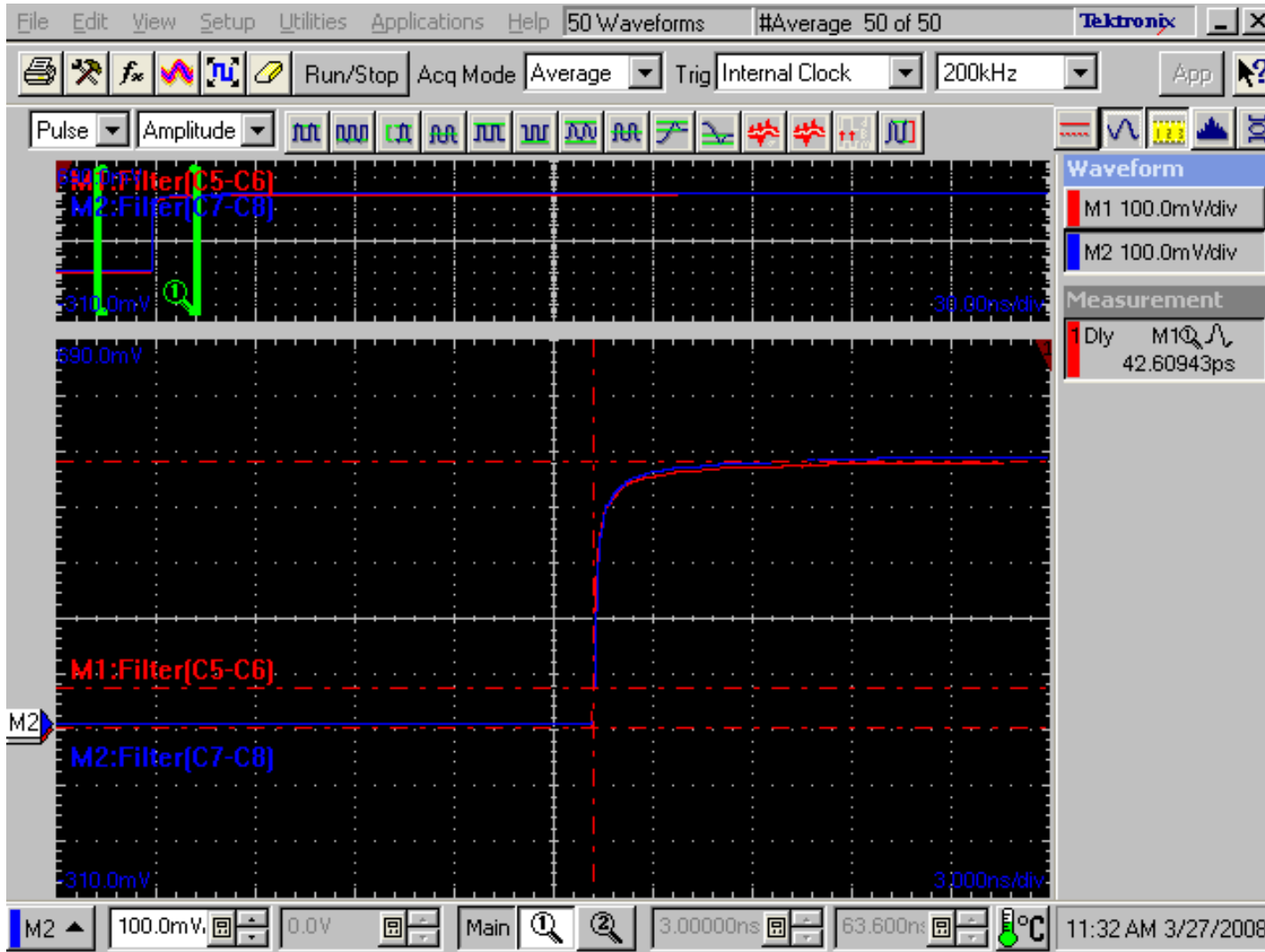


DisplayPort receptacle and Receptacle Calibration boards. *(not to scale)*

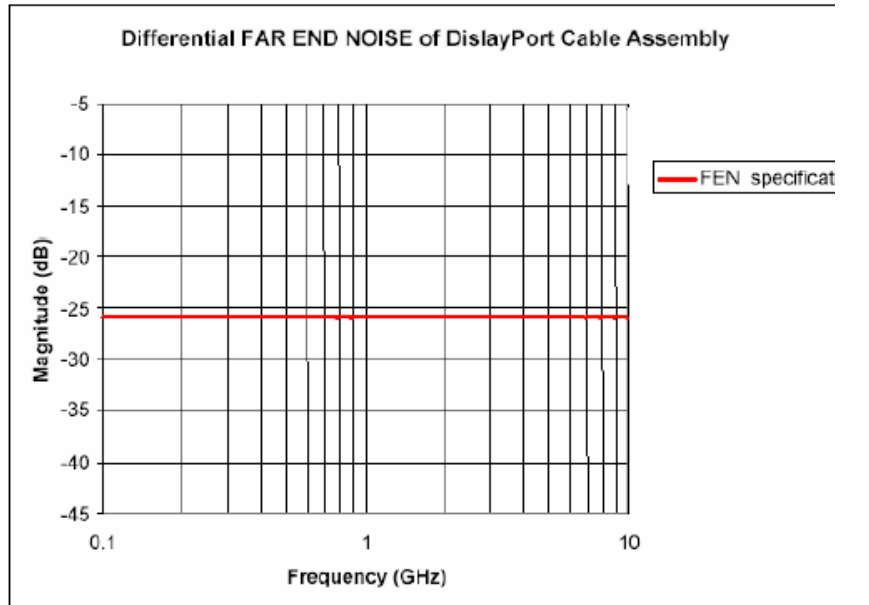
5.1 Cable Assembly Inter-pair Skew Measurements (Informative)



5.1 Cable Assembly Inter-pair Skew Measurements Example

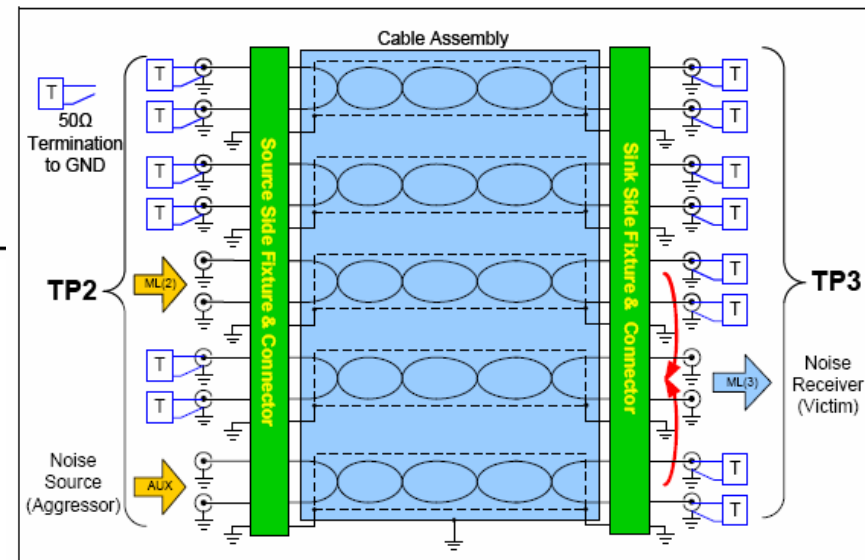


5.3 Far End Noise (FEN) Measurements (Normative)

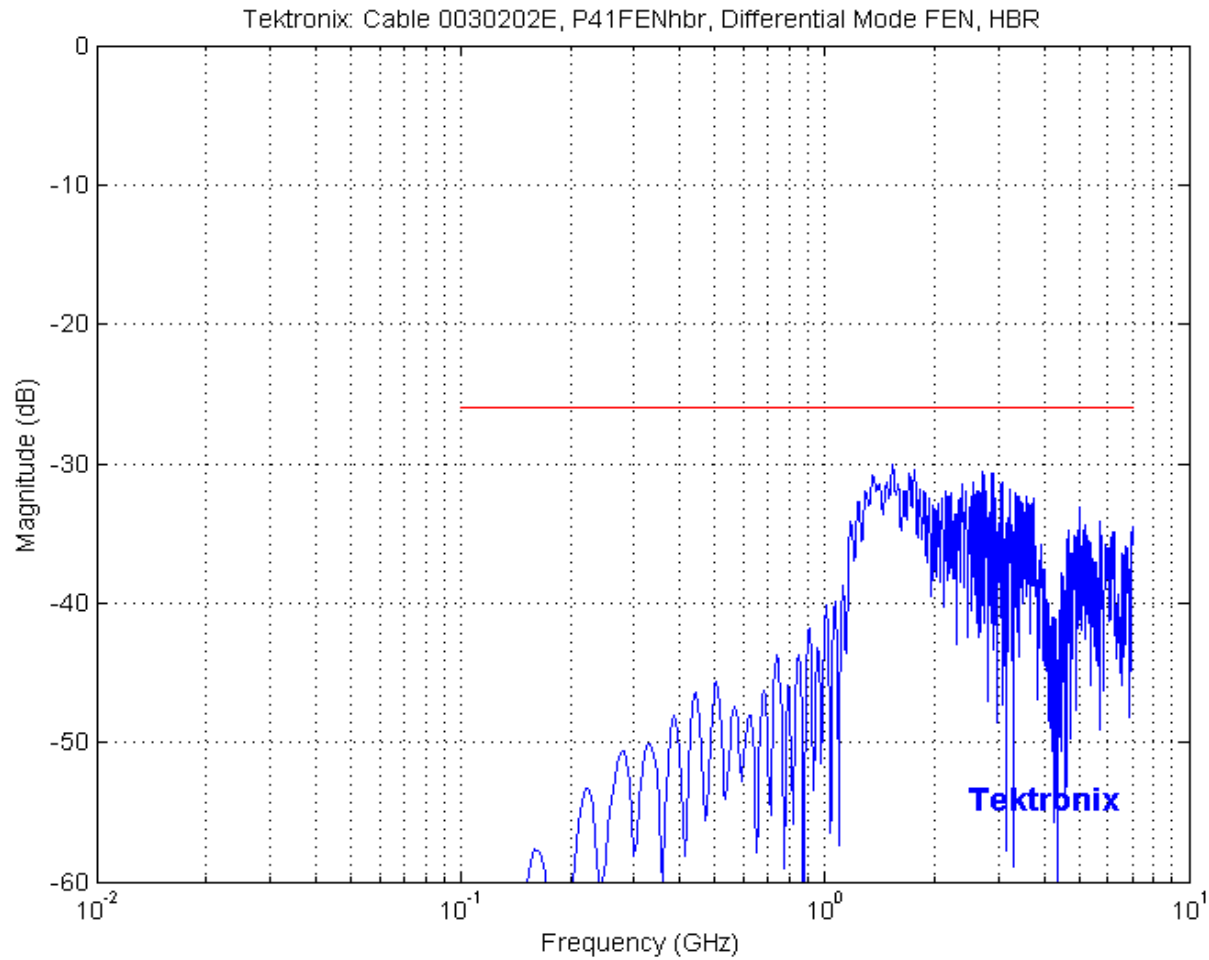


Summation of the crosstalk is required

Test #	Aggressor(s) Channel(s)	Victim Channel
1	Main Link(1)	Main Link(0)
2	Main Link(0) + Main Link(2)	Main Link(1)
3	Main Link(1) + Main Link(3)	Main Link(2)
4	Main Link(2) + AUX Ch.	Main Link(3)
5	Main Link(3)	AUX Ch.



5.3 Far End Noise (FEN) Measurements Example



5.4 Bulk Cable and Connector Impedance Measurements (Normative)

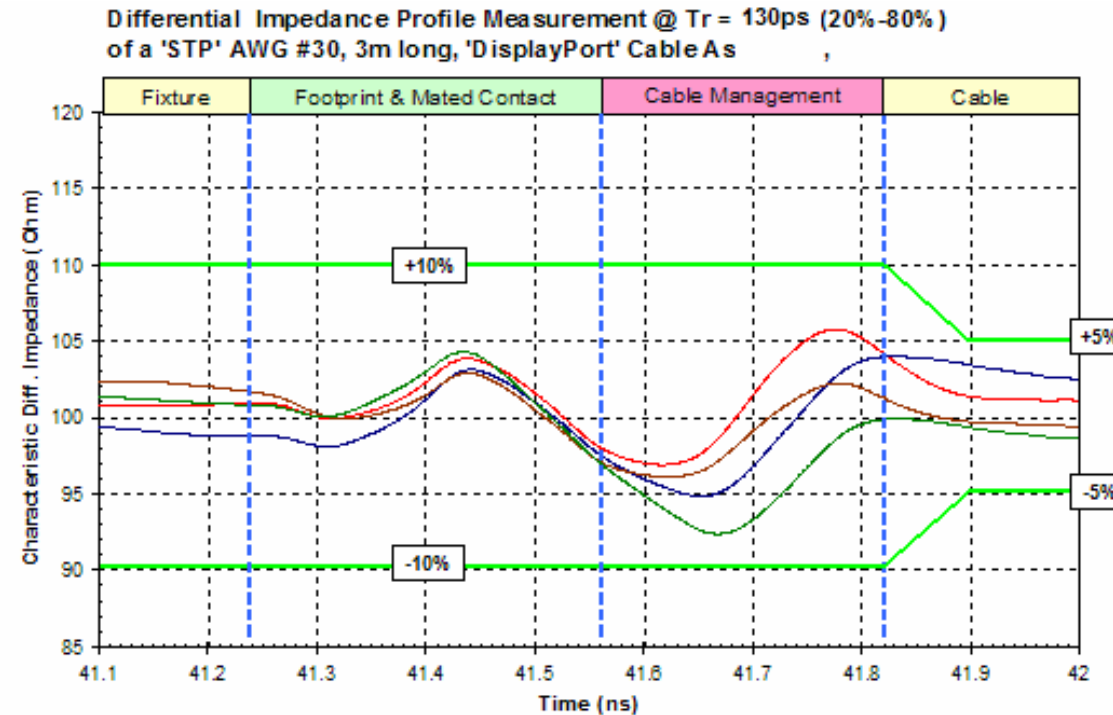
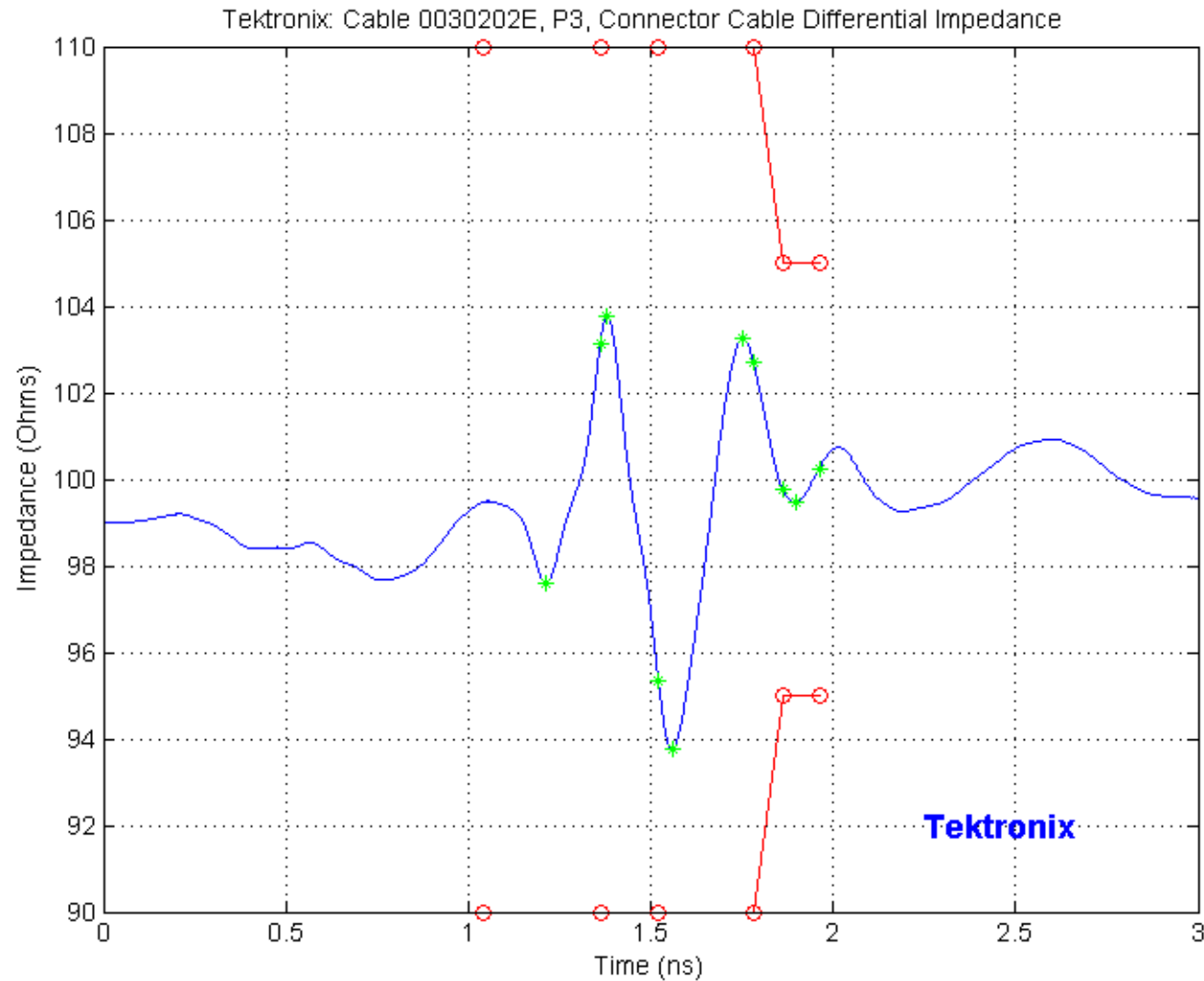


Table 4-1: Impedance Profile Values for Cable Assembly

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100 Ω	$\pm 10\%$	Fixture shall have traces lengths of no more than 50 mm (2")
Connector	100 Ω		
Wire Management	100 Ω		Transition from $\pm 10\%$ to $\pm 5\%$ shall have a slope of 5 Ω / 80ps
Cable	100 Ω		

5.4 Bulk Cable and Connector Impedance Measurements Example



5.5 Insertion Loss (IL/SDD21) Measurements (Normative); HBR

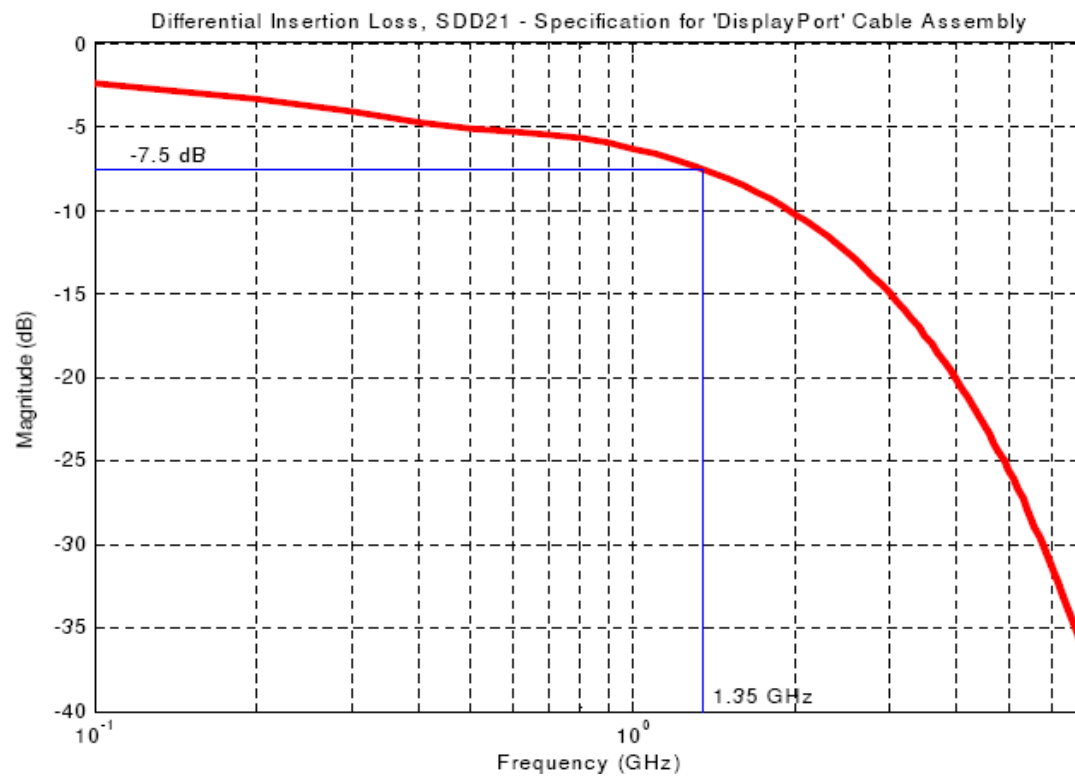
4.1.5.1.1 Insertion Loss Lower Limit for High Bit Rate Cable Assemblies

$$IL_{\min} [dB] = \begin{cases} -8.7 \times \sqrt{\frac{f}{f_0}} & ; 0.1 < f \leq \frac{f_0}{3} \\ 8.78\sqrt{f} - 7.54 * f - 7.52 & ; \frac{f_0}{3} < f \leq 7 \end{cases}$$

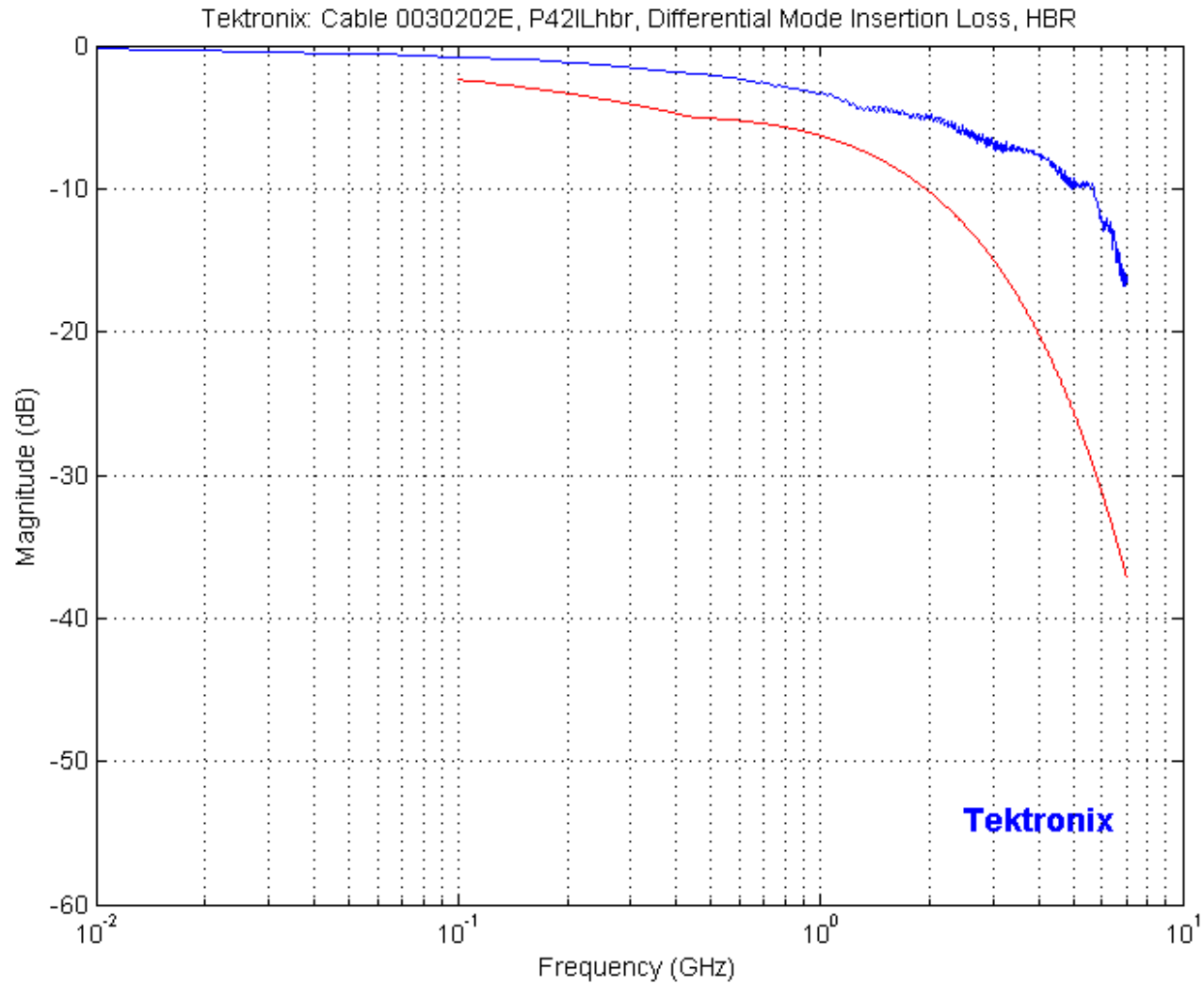
Where:

f is given in GHz

$f_0 = 1.35$ GHz



5.5 Insertion Loss (IL/SDD21) Measurements (Normative); HBR



DisplayPort Cable Automation Script

The screenshot shows the 'DisplayPort Cable' software window. The title bar reads 'DisplayPort Cable' and the version is 'v 1.0.4'. The interface is divided into several sections:

- Calibration:** A table with four columns for Port 1, Port 2, Port 3, and Port 4. Each column has a 'Deskew' row with channel labels (Ch 1-2, Ch 3-4, Ch 5-6, Ch 7-8) and an 'Odd (%)' row with a text input field set to '0.00'. Below this is a 'Zo (Ohm)' row with four text input fields, each set to '100'. At the bottom of this section are 'Trise (10-90%):' with a text input '180' and 'ps', and 'Threshold:' with a text input '45' and '%'. Below the calibration section is a 'Navg:' dropdown menu set to '500'.
- Acquisition and Analysis:** A section with three radio buttons: 'References', 'DUT', and 'Analysis'. The 'Analysis' radio button is selected.
- Buttons:** At the bottom are three buttons: 'OK' (green), 'Help' (yellow), and 'Close' (red).

The screenshot shows the 'WizardDutName' software window. The title bar reads 'WizardDutName'. The main text says 'Enter the cable length, lanes, and DUT name and click OK.' The interface includes:

- Cable length:** A group box with four radio buttons: '< 3m' (selected), '3m - 7m', '7m -15m', and '> 15m'.
- Lanes for ports 1 & 3:** A group box with five radio buttons: 'AUX' (selected), 'ML3', 'ML2', 'ML1', and 'ML0'.
- Lanes for ports 2 & 4:** A group box with five radio buttons: 'AUX', 'ML3' (selected), 'ML2', 'ML1', and 'ML0'.
- DUT Name:** A text input field containing 'testCable'.
- Buttons:** 'OK' and 'Cancel' buttons at the bottom.



Additional Resources

- <http://www.displayport.org>
- <http://www.tektronix.com/displayport>
- High-bandwidth Digital Content Protection
 - <http://www.digital-cp.com/>
- Video Electronics Standards Association
 - www.vesa.org